ABSTRACT OF THE DISCLOSURE

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In a flash memory, a threshold voltage of a memory transistor is decreased quickly by increasing a rising speed of a pulse voltage of an erasing pulse signal train during the first period of an erasing operation. In response to the threshold voltage of the memory transistor becoming lower than a threshold voltage of a reference transistor, the threshold voltage of the memory transistor is decreased slowly by reducing the rising speed of the pulse voltage of the erasing pulse signal train. Therefore, the erasing time can be reduced and depletion of the memory transistor can be prevented.